MetaSyn™

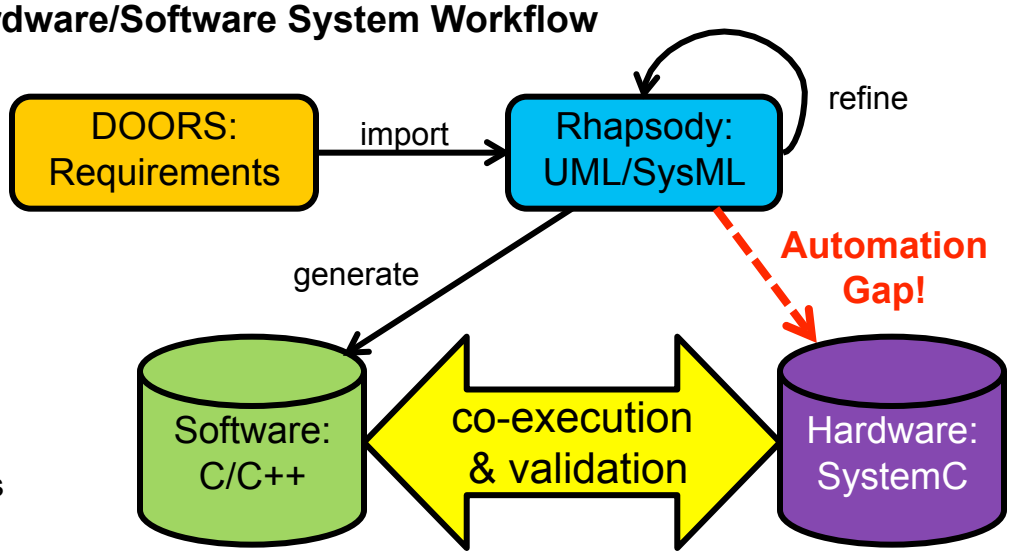
Rhapsody™/SysML Synthesis to SystemC

The development of embedded and computing systems has become quite complex. Time-to-market pressures, multiple dimensions of design trade-offs, quality, safety and reliability all factor in, as well as overall cost. Rational Rhapsody from IBM is a proven system design tool. But, there's still a need to facilitate an automated flow from Rhapsody's SysML description to both software and hardware implementation. MetaSyn, from innovative startup ExperMeta, provides that bridge. MetaSyn's SysML to SystemC synthesis enables flows for architectural trade-offs, for hardware synthesis, and for software simulation on virtual platforms.

Electronic systems have incredible time-to-market requirements. As software content increases, and hardware nodes move ever-downward, automated flows starting at higher levels of abstraction are the only way to successfully build systems. Software development must begin earlier in the project, as well as hardware verification. More architectural trade-offs are required to achieve an optimum balance between speed, power, weight, functionality and cost. Rhapsody is an established system design tool. Combining MetaSyn with Rhapsody enables automation from system design to hardware and software.

Hardware/Software System Workflow

In the system workflow, requirements are captured in DOORS, then imported into Rhapsody. Rhapsody can automatically generate software, but not hardware descriptions. The hardware models are needed to work with tools for architectural analysis/optimization, hardware implementation, and software simulation and validation. ExperMeta's MetaSyn bridges this *Automation Gap* in the flow.



Automated Generation of SystemC Models Critical to Successful Flow

- Leverage SysML executable models and validation
- Quicken availability of domain-appropriate models for software and hardware development
- Ensure consistency with Systems Engineering perspective
- Reduce errors introduced through manual SystemC creation
- Easily propagate top-level changes to lower levels

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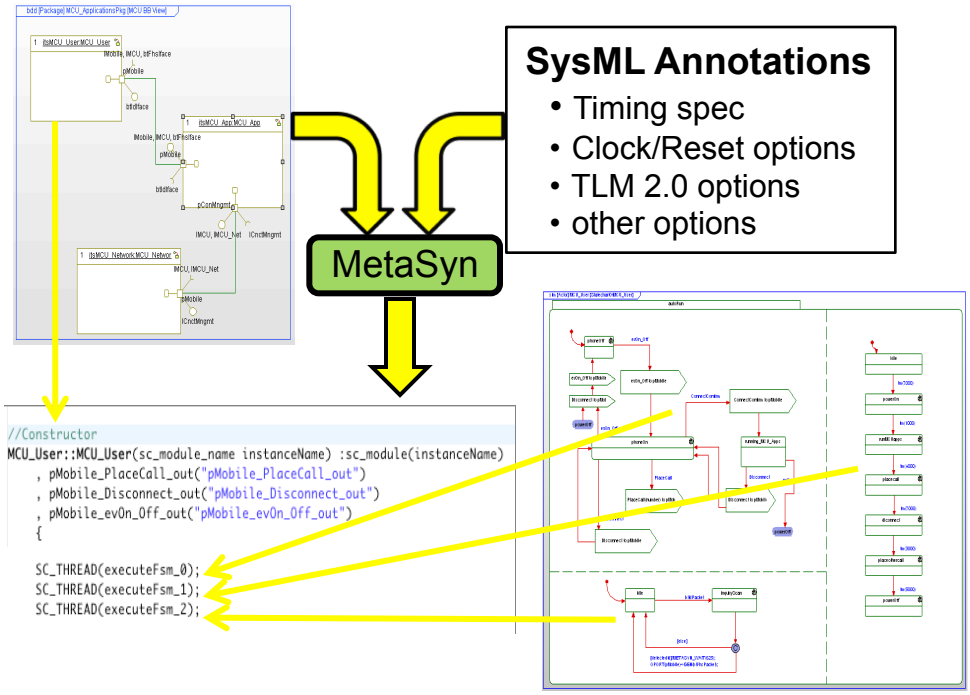
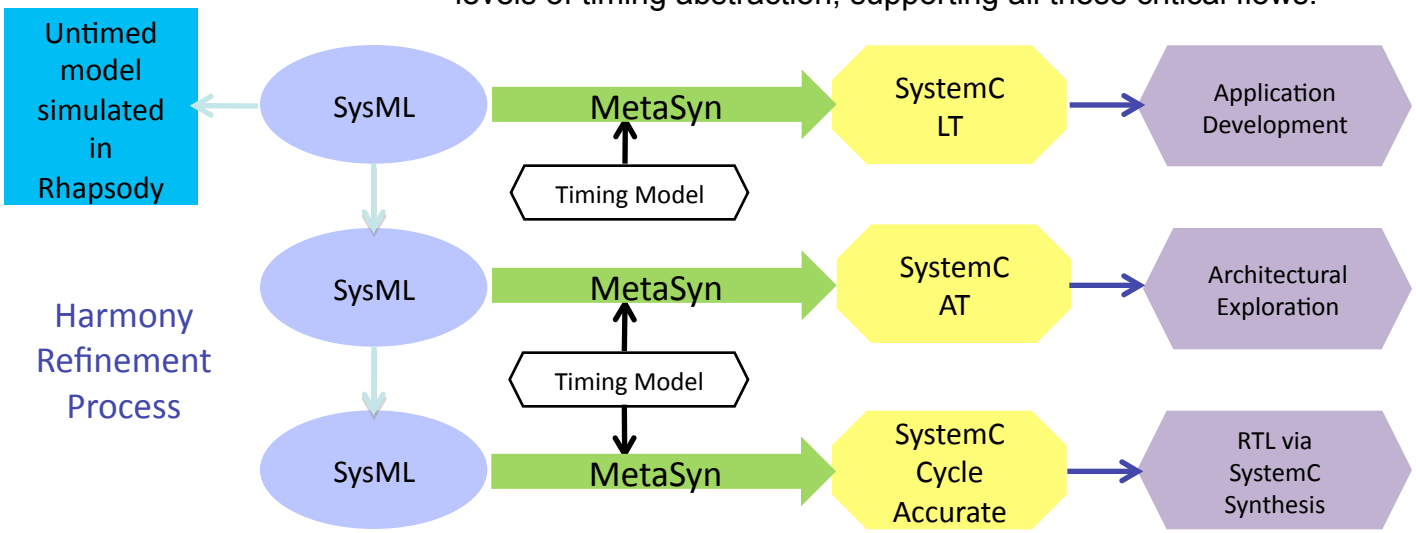
Rhapsody/SysML Synthesis → SystemC

SysML in Rhapsody is untimed and sequential, so how does MetaSyn generate cycle accurate, concurrent descriptions in SystemC? MetaSyn bridges the execution semantics by its sophisticated synthesis engine. MetaSyn's technology coordinates the parallel execution and guarantees preservation of transaction order, something that a naïve translation cannot. SysML structure is mapped to SystemC modules, state machine behavior is mapped to SystemC component structures, and AND-state concurrency is mapped to multiple SystemC processes within a block. Also, timing and hardware specific artifacts such as clock/reset lines are automatically generated.



Hardware, Software Flows with SystemC

SystemC is a C++ library with various levels of timing abstraction. Loosely timed (LT) models can be used in very fast software simulations for application validation. Approximately timed (AT) models are often used for architectural exploration. And cycle accurate models can be used either as a starting point for synthesis to RTL, or as a reference model for functional verification of manually generated RTL. MetaSyn can generate SystemC at all levels of timing abstraction, supporting all these critical flows.



ExperMeta

www.ExperMeta.com